

REMARKS

The Office Action of September 8, 2010, was received and carefully reviewed. Claims 6, 8-14, 17-22, 24-27, 29, 47-50 and 55-59 remain currently pending for consideration.

Claim Rejections Under 35 U.S.C. § 103

Claims 18, 19, 22 and 49 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,471,225 to Parks (“Parks”), in view of Japanese Pat. App. Pub. No. JP 58-143389 to Hoshi (“Hoshi”). Claims 6, 8, 11, 47 and 55-59 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Parks, in view of U.S. Patent No. 5,325,338 to Runaldue et al. (“Runaldue”), and further in view of Hoshi. Claims 9 and 10 stand rejected under §103(a) as being unpatentable over Parks in view of Runaldue, and further in view of Hoshi and U.S. Patent No. 5,196,839 to Johary et al. (“Johary”). Claims 12-14, 17, 20, 21, 24-27, 29, 48 and 50 stand rejected under §103(a) as being unpatentable over Parks in view of Hoshi, and further in view of Johary. These rejections are traversed for the reasons advanced in detail below.

The invention cited in the currently pending claims include a combination of features that are not disclosed by the cited reference noted above for the reasons advanced in detail in the prior response, those reasons being incorporated herein by reference. Further, addressing the Office Action of September 8, 2010, on pages 3-4, 6 and 14 thereof, the Examiner asserts that Hoshi discloses the limitation, “wherein an AC voltage having an amplitude equivalent to that of the voltages output of the memory circuit is supplied to the opposite electrode”, as is recited in independent claims 6, 12, 18, 24, 55 and 57. Specifically, the Examiner asserts that reference numeral 12a of FIG. 3A corresponds to the AC voltage, and that reference numeral 12b of FIG. 3A corresponds to the voltages output of the memory circuit.¹ Applicant respectfully disagrees.

Despite the assertions by the Examiner, Parks, Hoshi, Runaldue and/or Johary, taken alone or in combination, fail to disclose, suggest or render obvious at least an AC voltage having an amplitude equivalent to that of the voltages output. For example, reference

¹ On pages 3, 6 and 14 of the Office Action, the Examiner refers to reference numeral 12a of FIG. 3A and reference numeral 12b of FIG. 3B. However, reference numeral 12b is not included in FIG. 3B, and is only included in FIG. 3A. Applicant understands that this was a typographical error, and that the Examiner intended to refer to reference numeral 12b of FIG. 3A. Clarification is respectfully requested from the Examiner should this understanding be incorrect.

numeral 12b of FIG. 3A of Hoshi, which the Examiner relates to the voltages output of the memory circuit of the claimed invention, is actually an output of the signal selection circuit 8. *See page 5, lines 19-29, of the translation of Hoshi*. Hoshi is silent as to an amplitude of the outputs of memory circuit 7. The Examiner readily admits that Parks also fails to disclose this feature of the claimed invention. *See pages 3, 6 and 14 of the Office Action*. Runalduie, cited by the Examiner as allegedly disclosing each inverter comprising both an N-channel and P-channel TFT, and Johary, cited as allegedly disclosing a time gradation display device, also fail to overcome this deficiency of Hoshi.

Thus, Applicant respectfully requests reconsideration and withdrawal of the rejection of independent claims 6, 12, 18, 24, 55 and 57. The rejection of dependent claims 8-11, 13, 14, 17, 19-22, 25-27, 29, 47-50 and 56, 58 and 59 is believed to be improper at least by virtue of their dependency on claims 6, 12, 18, 24, 55 or 57.

In view of the foregoing, Applicant respectfully requests reconsideration and allowance of the instant application. If a conference would be helpful in expediting prosecution of the instant application, the Examiner is invited to telephone the undersigned to arrange such a conference.

Respectfully submitted,

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